What is Claimed is:

1. A grid array microelectronic package comprising:

a substrate; and

an array of external connectors on the substrate that are arranged in a plurality of rows and a plurality of columns to define a periphery of the array and an interior of the array; and

a routing channel in the array that increases the periphery of the array by at least four external connectors compared to absence of the routing channel.

2. A package according to Claim 1 wherein the routing channel comprises at least two missing external connectors in the array.

3. A package according to Claim 1 wherein the array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

4. A package according to Claim 1 further comprising a plurality of signal conductors that extend along the routing channel.

5. A package according to Claim 1 wherein the substrate is a first substrate and wherein the array of external connectors is a first array of external connectors, the package further comprising:

a second substrate; and

a second array of external connectors on the second substrate that are arranged to mate with the first array of external connectors.

6. A package according to Claim 5 wherein the second array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the second substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

7. A package according to Claim 1 wherein the plurality of rows is N rows, wherein the plurality of columns is M columns and wherein the periphery, Cp, of the array that includes the routing channel therein is defined by:

$$Cp \geq 2N + 2M.$$

8. A grid array microelectronic package comprising:

a substrate; and

an array of external connectors on the substrate that are arranged in at least four rows and at least four columns, including a pair of peripheral rows and a pair of peripheral columns at a periphery thereof and at least one pair of interior rows and at least one pair of interior columns between the respective pair of peripheral rows and peripheral columns, wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are missing from the array to define a routing channel that extends from the periphery of the array towards the interior of the array.

9. A package according to Claim 8 wherein a first external connector in a peripheral row or peripheral column, a second external connector in a first interior row or first interior column adjacent the peripheral row or peripheral column and a third external connector in a third interior row or third interior column adjacent the first interior row or first interior column and remote from the peripheral row or peripheral column are missing from the array to define the routing channel that extends from the periphery of the array towards the interior of the array.

10. A package according to Claim 8 wherein the array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

11. A package according to Claim 8 further comprising a plurality of signal conductors that extend along the routing channel.

12. A package according to Claim 8 wherein the substrate is a first substrate and wherein the array of external connectors is a first array of external connectors, the package further comprising:

a second substrate; and

a second array of external connectors on the second substrate that are arranged to mate with the first array of external connectors.

13. A package according to Claim 12 wherein the second array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the second substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

14. A grid array microelectronic package comprising:

a substrate; and

an array of external connectors on the substrate that are arranged in at least four rows and at least four columns, including a pair of peripheral rows and a pair of peripheral columns at a periphery thereof and at least one pair of interior rows and at least one pair of interior columns between the respective pair of peripheral rows and peripheral columns, wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array.

15. A package according to Claim 14 wherein a first external connector in a peripheral row or peripheral column, a second external connector in a first interior row or first interior column adjacent the peripheral row or peripheral column and a third external connector in a third interior row or third interior column adjacent the first interior row or first interior column and remote from the peripheral row or peripheral column are electrically strapped together to define the routing channel that extends from the periphery of the array towards the interior of the array.

16. A package according to Claim 14 wherein the array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the

substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

17. A package according to Claim 14 further comprising a plurality of signal conductors that extend along the routing channel.

18. A package according to Claim 14 wherein the substrate is a first substrate and wherein the array of external connectors is a first array of external connectors, the package further comprising:

a second substrate; and

a second array of external connectors on the second substrate that are arranged to mate with the first array of external connectors.

19. A package according to Claim 18 wherein the second array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the second substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

20. A grid array microelectronic package comprising:

a substrate; and

an array of external connectors on the substrate that are arranged in at least four rows and at least four columns, including a pair of peripheral rows and a pair of peripheral columns at a periphery thereof and at least one pair of interior rows and at least one pair of interior columns between the respective pair of peripheral rows and peripheral columns, wherein at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are operationally disconnected from the substrate to define a routing channel that extends from the periphery of the array towards the interior of the array.

21. A package according to Claim 20 wherein a first external connector in a peripheral row or peripheral column, a second external connector in a first interior row or first interior column adjacent the peripheral row or peripheral column and a third external connector in a third interior row or third interior column adjacent the

first interior row or first interior column and remote from the peripheral row or peripheral column are operationally disconnected from the substrate to define the routing channel that extends from the periphery of the array towards the interior of the array.

22. A package according to Claim 20 wherein the array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.

23. A package according to Claim 20 further comprising a plurality of signal conductors that extend along the routing channel.

24. A package according to Claim 20 wherein the substrate is a first substrate and wherein the array of external connectors is a first array of external connectors, the package further comprising:

a second substrate; and

a second array of external connectors on the second substrate that are arranged to mate with the first array of external connectors.

25. A package according to Claim 24 wherein the second array of external connectors comprises an array of pads, pins, balls and/or bumps and wherein the second substrate comprises an integrated circuit, a ceramic substrate, a plastic substrate and/or a printed circuit board.